WHAT IS CLAIMED IS:

1. A method of processing first and second received packets of real-time information, comprising the steps of:

computing for each of said received packets respective deadline intervals; and

ordering processing of the first and second received packets according to the respective deadline intervals.

2. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals.

3. The method of claim 1 further comprising temporarily storing on a link list information about the packets including the respective deadline intervals.

4. The method of claim 1 further comprising temporarily storing on a link list information about the packets including the respective deadline intervals, storing real-time information contained in the packets in a separate storage area, and also temporarily storing on the link list respective pointers associated with the respective deadline intervals, the pointers pointing to the real-time information in the separate storage area from the respective packets.

5. The method of claim 1 wherein further packets arrive and further comprising computing for each futher packet a respective deadline interval from a packet arrival

time and packet sequence number and the clock time and then ordering processing of the packets according to the respective deadline intervals.

6. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals, and periodically decrementing the deadline intervals as time passes.

7. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals, and wherein a further packet arrives and then computing for the further packet a further deadline interval and sorting the queue to insert information about the further packet on the queue in order of its further deadline intervals relative to the respective deadline intervals already on the queue.

8. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals adjusted for passage of time.

9. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals adjusted for passage of time, and discarding packets for which the deadline has passed.

10. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals, and decoding a packet having the shortest time to deadline as expressed by its deadline interval.

11. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective deadline intervals, decoding a packet having the shortest time to deadline as expressed by its deadline interval, and updating the queue to substantially remove the information pertaining to that packet from the queue.

12. The method of claim 1 wherein the packets include real-time information encoded in frames having a frame size, and the method further comprising temporarily storing information about the packets on a queue, the information comprising frame size respective to the packets.

13. The method of claim 1 wherein the packets include real-time information encoded according to an identifiable coding process, and the method further comprising temporarily storing information about the packets on a queue, the information comprising an identifier of the identifiable coding process respective to the packets.

14. The method of claim 1 further comprising generating information about the packets in the form of primary and secondary keys and temporarily storing information about

the packets on a queue in order of the primary keys, and for packets having identical primary keys storing them in order of the secondary keys.

15. The method of claim 1 further comprising generating information about the packets in the form of primary keys comprising deadline intervals and secondary keys comprising frame sizes, and temporarily storing information about the packets on a queue in order of the primary keys, and for packets having identical primary keys storing them in order of the secondary keys.

16. The method of claim 1 for use in a system having plural egress channel buffers into which arriving packets are distributed by channel whereby reserves in the egress channel buffers occur, the method further comprising generating information about the packets in the form of primary keys comprising deadline intervals and secondary keys comprising sizes of reserve in the egress channel buffers, and temporarily storing information about the packets on a queue in order of the primary keys, and for packets having identical primary keys storing them in order of the secondary keys.

17. The method of claim 1 wherein the step of computing deadline intervals includes computing the deadline intervals from a packet arrival time and packet sequence number and a clock time.

18. The method of claim 1 wherein the step of computing deadline intervals includes computing such that for an arriving packet the deadline interval DI is the difference between an arrival time A of the arriving packet and a deadline time D.

19. The method of claim 1 wherein the step of computing deadline intervals includes computing wherein for an arriving packet the deadline interval DI is the difference between an arrival time A of the arriving packet and a deadline time D rounded down to the nearest unit of a predetermined frame time width.

20. The method of claim 1 wherein the step of computing deadline intervals includes a step for an arriving packet j having a sequence number Sj and frame width F of determining a deadline time Dj for the arriving packet j from a deadline Di previously determined for an earlier packet i having a sequence number Si substantially by determining a product F multiplied by a number (Sj – Si – 1) and adding the product to the deadline Di.

21. The method of claim 1 wherein the step of computing deadline intervals includes steps for an arriving packet j having a sequence number Sj and frame width F of

determining a deadline time Dj for the arriving packet j from a deadline Di previously determined for an earlier packet i having a sequence number Si substantially by determining a product F multiplied by a number (Sj – Si – 1) and adding the product to the deadline Di; and

producing a representation ofj the deadline interval DI substantially as a difference between an arrival time A of the arriving packet less the deadline Dj for the arriving packet.

22. The method of claim 1 wherein the step of computing deadline intervals includes computing for an arriving packet i a deadline Di by

storing a time value To for a beginning packet of a stream; and

continually incrementing the stored time value To by an amount representing a frame size F to obtain the deadline Di.

23. The method of claim 1 wherein the step of computing deadline intervals includes computing, for an arriving packet i as ith packet in a stream, a deadline Di by

storing a time value To for a beginning packet of a stream; and

producing a deadline Di substantially as (To + (i-1)F)]; and

generating a deadline interval DI for arriving packet i substantially as a latest packet i time of arrival Ai less the deadline Di.

24. The method of claim 1 wherein the step of computing deadline intervals includes computing, for an arriving packet i as ith packet in a stream having frame width F, and for an arriving packet j as jth packet in the stream, a pair of deadlines Di and Dj by

storing a time value To for a beginning packet of a stream; and

producing the deadline Di substantially as (To + (i-1)F)]; and

determining the deadline Dj for the arriving packet j from the deadline Di substantially according to $Dj = Di + (Sj - Si - 1)F$.

25. The method of claim 1 wherein the step of computing deadline intervals includes computing, for an arriving packet i as ith packet in a stream having frame width F, and for an arriving packet j as jth packet in the stream, a pair of deadline intervals DIi and DIj from respective arrival times Ai and Aj by

storing a time value To for a beginning packet of a stream; and

producing the deadline interval DIi substantially according to

$$DIi = Ai - (To + (i-1)F); \text{ and}$$

determining the deadline interval DIj substantially according to

$$DIj = Aj - (To + (i-1)F) - (Sj - Si - 1)F.$$

26. The process of claim 1 further comprising sorting information from the packets in order of the deadline intervals, the ordering of the processing being responsive to said sorting.

27. The process of claim 1 further comprising sorting information from the packets in order of the deadline intervals, and further sorting within the deadline intervals according to a secondary key, the ordering of the processing being responsive to said sorting.

28. The process of claim 1 further comprising sorting information from the packets in order of the deadline intervals, and further sorting within the deadline intervals according to a secondary key that takes into account the amount of time that a decoder takes to work, the ordering of the processing being responsive to said sorting.

29. The method of claim 1 wherein the step of computing deadline intervals includes steps, for an arriving silence packet j representing a number of silence frames S having a frame width F, of determining a deadline interval DIj for the arriving silence packet j from a deadline interval DIi previously determined for an earlier packet I, substantially according to DIj = DIi + SxF, in other words as the sum of the deadline interval DIi added to a product of the number of silence frames S times the frame width F.

30. A method of processing packets from streams of real-time information in communications channels fed to buffers respective to the communications channesl and accumulating information in reserves in the buffers, comprising the steps of:

computing for the buffers respective sizes of their respective reserves; and

ordering processing of the packets according to a priority depending at least in part on the sizes of the respective reserves.

31. The method of claim 30 further comprising temporarily storing information about the packets on a queue in order of the respective sizes of the respective reserves.

32. The method of claim 30 further comprising temporarily storing information about the packets on a queue in order of the respective sizes of the respective reserves.

33. The method of claim 30 further comprising temporarily storing information about the packets on a queue in order of the respective sizes of the respective reserves, and wherein a further packet arrives in a given channel and then sorting the queue to insert information about the further packet on the queue in order of the size of the reserve in the buffer for the given channel.

34. The method of claim 30 further comprising temporarily storing information about the packets on a queue in order of the respective sizes of the respective reserves and resorting the queue as the reserves change in size over time.

35. The method of claim 1 further comprising temporarily storing information about the packets on a queue in order of the respective sizes of reserves, the information for each packet including a deadline for using that particular packet, and discarding packets for which the deadline has passed.

36. The method of claim 30 wherein the packets include real-time information encoded in frames having a frame size, and the method further comprising temporarily storing information about the packets on a queue, the information comprising frame size respective to the packets.

37. The method of claim 30 wherein the packets include real-time information encoded according to an identifiable coding process, and the method further comprising temporarily storing information about the packets on a queue, the information comprising an identifier of the identifiable coding process respective to the packets.

38. The method of claim 30 further comprising generating information about the packets in the form of primary and secondary keys and temporarily storing information about the packets on a queue in order of the primary keys, and for packets having identical primary keys storing them in order of the secondary keys.

39. A method of processing a received packet of real-time information, comprising the steps of:

extracting a packet deadline for the received packet;

placing the packet in an egress scheduling list according to its deadline; and

updating the egress scheduling list as packets are utilized and as deadlines pass.

40. The method of claim 39 further comprising delaying processing of the received packet according to its position on the egress scheduling list.

41. A method of processing a received packet of real-time information, comprising the steps of:

extracting a packet deadline interval DI of time-to-deadline for the received packet;

placing the packet in an egress scheduling list according to its deadline interval DI; and

updating the egress scheduling list by periodically decrementing the deadline interval DI for the packet.

42. The method of claim 41 further comprising delaying processing of the received packet according to its position on the egress scheduling list.

43. The method of claim 41 further comprising decoding packets and executing the extracting, placing, updating, and decoding steps substantially non-preemptively.

44. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and executing the extracting, placing, updating, and egress packet decoding and ingress packet processing steps substantially non-preemptively.

45. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting ingress packet processing by any of the extracting, placing, updating, and egress packet decoding steps.

46. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting ingress packet processing by either of the

placing and egress packet decoding steps to be performed on an egress packet, except when the deadline interval of the egress packet has expired.

47. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting ingress packet processing by either of the placing and egress packet decoding steps to be performed on an egress packet, when the deadline interval for the egress packet lies between expiration and a predetermined value.

48. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting egress packet processing of a first egress packet having a deadline interval exceeding a value, by preemptively executing either of the placing and egress packet decoding steps on a second egress packet, wherein the deadline interval for the second egress packet lies between expiration and the value.

49. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting egress packet processing of an egress packet having a deadline interval exceeding a value, by preemptively executing ingress packet processing of at least one ingress packet.

50. The method of claim 41 further comprising executing egress packet processing of a first egress packet having a first deadline interval less than a first value and greater than a second value, and preempting the execution of the egress packet processing of

the first egress packet by preemptively executing egress packet processing of a second egress packet having a deadline interval less than the second value.

51. The method of claim 41 further comprising egress packet decoding and ingress packet processing, and preempting ingress packet processing by preemptively executing egress packet processing of a first egress packet having a first deadline interval less than a first value and greater than a second value, and preempting the execution of the egress packet processing of the first egress packet by preemptively executing egress packet processing of a second egress packet having a deadline interval less than the second value.

52. A method of processing first and second received packets of real-time information from different communications channels, comprising the steps of: extracting a packet deadline interval DI of time-to-deadline for each received packet;

placing the packet in an egress scheduling list according to its deadline interval DI; and

decoding the packets according to a priority depending to their deadline intervals.

53. The process of claim 52 wherein the channels have decoders operating on at substantially coincident frame boundaries whereby a same-deadline process is executed.

54. The process of claim 52 wherein the channels have decoders operating on non-coincident frame boundaries whereby a staggered-deadline process is executed.

55. A method of processing first and second received packets of real-time information from different communications channels wherein the channels have decoders operating on non-coincident frame boundaries whereby a staggered-deadline process is executed, and wherein the first packet has a first deadline and is currently in decode while the second packet is just-arriving and has a second deadline earlier than the first deadline, and the process comprises testing to determine whether both the second and first packets can be decoded ahead of their respective deadlines if the second packet were decoded preemptively, and if so, then preempting processing the first packet and preemptively executing decode of the second packet.

56. The method of claim 55 further comprising initiating a timer upon beginning of decode of the first packet, and performing the testing step responsive to the timer.

57. The method of claim 55 further comprising initiating respective channel counters respective to decodes of packets including the first packet, selecting a channel counter, and performing the testing step responsive to a the selected channel counter.

58. The method of claim 55 further comprising executing a decode process including steps of partial decoding of the first packet interspersed with at least one break process, and performing the testing step responsive to the at least one break process.

59. The method of claim 55 further comprising bypassing the testing step responsive to a bypass flag indicative of a higher priority channel.

60. A method of processing egress information and of executing an ingress process wherein the egress information has a value of lowest first deadline interval DI, and the method comprises preemption by the ingress process when the value of lowest first deadline interval DI of the egress information exceeds a predetermined amount K.

61. The method of claim 60 wherein an egress packet subsequently arrives, and the method comprises determining a second deadline interval for the arriving egress packet, and when the second deadline interval is less than a value, then preempting the ingress process.

62. The method of claim 60 wherein an egress packet subsequently arrives, and the method comprises determining a second deadline interval for the arriving egress packet, and when the second deadline interval is less than the predetermined amount K, then preempting the ingress process to process the arriving egress packet.

63. A method of processing received packets of real-time information in channels having various channel deadlines Di, comprising:

electronically putting values representative of the channel deadlines Di in an order of urgency;

launching decode execution of a first received packet having an early channel deadline;

detecting absence of a second packet having a second next most urgent channel deadline but presence of a third packet having a third next most urgent channel deadline;

launching decode execution said third packet whereupon the second packet arrives;

generating a value indicating whether sufficient time exists to save the second packet, and if so, then preempting the now-underway decode execution of the third packet to save the second packet.

64. The method of claim 63 further comprising returning to the point where decode execution of the third packet was preempted , whereupon decode execution of the third packet proceeds to completion.

65. The method of claim 63 further comprising testing to determine whether the third packet can be decoded ahead of its deadlines if the second packet were decoded preemptively, and if so, then preempting processing of the third packet and preemptively executing decode of the second packet.

66. A method of processing a packet stream of arriving packets having packetized information, the method comprising:

detecting whether the arriving packets are respectively voice packets or silence packets;

queuing information from the voice packets;

decoding information from the voice packets to produce decoded voice information;

post-processing information from the silence packets; and

buffering the decoded voice information from the voice packets interspersed with post-processed information from the silence packets.

67. The method of claim 66 further comprising maintaining a scheduling list of information about the voice packets including respective deadline intervals responsive to information from the silence packets where such information is relevant to deadline interval of a voice packet.

68. The method of claim 66 further comprising performing the detecting step of determining whether the arriving packets are respectively voice packets or silence packets, prior to executing the step of queuing information from the voice packets.

69. The method of claim 66 wherein the queuing step also includes queuing the silence packets indiscriminately with the voice packets.

70. The method of claim 66 wherein the queuing step also includes queuing the silence packets indiscriminately with the voice packets, and wherein the detecting step of

determining whether the arriving packets are respectively voice packets or silence packets is performed after queuing.

71. The method of claim 66 wherein the queuing step also includes queuing the silence packets indiscriminately with the voice packets, and wherein the detecting step of determining whether the arriving packets are respectively voice packets or silence packets is performed during decoding.

72. A process of generating data descriptive of circular time differences between times of events A and B, the process comprising:

electronically subtracting a value representative of the time of event B from a value representative of the time of event A, there resulting a most significant bit (MSB); and

providing the MSB itself as a flag indicating which of events A and B is prior to the other.

73. A process of generating circular time differences between times of events A and B, the process comprising:

electronically subtracting and delivering to a storage element a value representative of the time of event B from a value representative of the time of event A, resulting in an electronic representation (delta) having a most significant bit (MSB) and a sign bit S; and

electronically processing the electronic representation (delta) and a predetermined value (TMAX) in response to the MSB and the sign bit S to generate the circular time difference.

74. The process of claim 73 wherein the electronically processing step includes four cases, wherein two of the cases do not alter the electronic representation (delta), and the other two cases combine the electronic representation (delta) with the predetermined value (TMAX).

75. The process of claim 73 wherein the electronically processing step includes four cases, wherein two of the cases do not alter the electronic representation (delta), a third one of the cases adds the electronic representation (delta) to the predetermined value (TMAX) , and a fourth case subtracts the predetermined value (TMAX) from the electronic representation (delta) to produce the circular time difference.

76. The process of claim 73 wherein the electronically processing step adds the electronic representation (delta) to the predetermined value (TMAX) provided the sign bit is positive and the MSB is zero.

77. The process of claim 73 wherein the electronically processing step subtracts the predetermined value (TMAX) from the electronic representation (delta) when the sign bit is positive and the MSB is one.

78. The process of claim 73 further comprising processing first and second received packets of real-time information by:

computing for each of said received packets respective deadline intervals as circular time differences between a respective deadline D and a respective packet arrival time A; and

ordering processing of the first and second received packets according to the respective circular time differences.

79. The process of claim 73 further comprising processing a received packet of real-time information by:

generating as a circular time difference a packet deadline interval DI of time-to-deadline for the received packet;

placing the packet in an egress scheduling list according to its deadline interval DI; and

updating the egress scheduling list by periodically decrementing the deadline interval DI for the packet.

80. The process of claim 73 further comprising processing first and second received packets of real-time information by:

computing for each of said received packets respective deadline intervals as circular time differences between a respective deadline D and a respective packet arrival time A;

placing the packet in an egress scheduling list according to its deadline interval DI; and

decoding the packets according to a priority depending to their circular time differences.

81. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an egress packet control establishing operations in the processor circuit generating for first and second received packets respective deadline intervals and ordering the processing in the processor circuit of the first and second received packets according to the respective deadline intervals.

82. A single-chip stream processor integrated circuit adapted to process packets from streams of real-time information in communications channels, the single-chip stream processor comprising:

a processing unit; and embedded electronic instructions comprising an egress packet control establishing egress channel buffers respective to the communications channels and further establishing operations in the processor unit streaming the packets to the channel buffers to accumulate information in reserves in the buffers, the operations establishing respective sizes of the respective reserves; and ordering processing of the packets in the processing unit according to a priority depending at least in part on the sizes of the respective reserves.

83. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the processor circuit that extract a packet deadline interval DI of time-to-deadline for a received packet, that further place the packet in the egress scheduling list according to its deadline interval DI, and that periodically decrement the egress scheduling list deadline interval DI.

84. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the processor circuit that extract a packet deadline intervals DI, place packets in the egress scheduling list according to deadline intervals DI; and embed a decoder that decodes the packets according to a priority depending to their deadline intervals.

85. A single-chip integrated circuit comprising:

a processor circuit; and embedded electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the processor circuit that establish channel decoders on non-coincident frame boundaries and a packet engine to detect when a first packet has a first deadline and is currently in decode while a second packet is just-arriving and has a second deadline earlier than the first deadline, and the packet engine establishes a determination whether both the second and first packets can be decoded ahead of their respective deadlines if the second packet

were decoded preemptively, and if so, then preempts the processor circuit channel decoder structure to decode the second packet.

86. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an ingress/egress packet control engine that processes egress information and determines lowest first egress deadline interval DI and further executes an ingress process preempting the egress process when the value of lowest first egress deadline interval DI exceeds a predetermined amount K.

87. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an ingress/egress packet control engine that processes egress channels having various channel deadlines Di, electronically orders channel deadlines Di by urgency, decodes a first egress packet having a deadline, detects absence of a second packet having a second next most urgent channel deadline but presence of a third packet having a third next most urgent channel deadline, launches decode of said third packet, and whereupon the second packet arrives, generates a value indicating whether sufficient time exists to save the second packet, and if so, preempts the now-underway decode execution of the third packet to save the second packet.

88. A single-chip integrated circuit comprising:

a processor circuit; and

embedded electronic instructions comprising an egress packet control engine that detects whether the arriving packets are respectively voice packets or silence packets, queues information from the voice packets and produces decoded voice information, post-processes the silence packets, and buffers the decoded voice information from the voice packets interspersed with post-processed silence packets.

89. A single-chip integrated circuit comprising:

storage for values representative of the time of two events;

a subtractor coupled to the storage and operative to generate a difference value (delta) and deliver the difference value into said storage thereby resulting a most significant bit (MSB) of the difference value (delta); and

a flag register having a bit fed with said MSB to indicating which of events A and B is prior to the other.

90. A single-chip circular time differencing integrated circuit comprising:

storage for values representative of the time of two events;

an adder/subtractor coupled to the storage and operative to generate an electronic difference (delta) and deliver the difference value into said storage thereby resulting a sign bit (S) and a most significant bit (MSB) of the difference value (delta); and

logic circuitry responsive to the MSB and the sign bit S of the electronic difference (delta) and a predetermined value (TMAX), the logic circuitry driving said adder/subtractor to generate the circular time difference of the two events.

91. The integrated circuit of claim 90 further comprising a voice codec and buffers coupled to said adder subtractor, storage, and logic circuitry.

92. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly providing voice over packet transmissions and embedded electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the integrated circuit that extract a packet deadline interval DI of time-to-deadline for a received packet, that further place the packet in the egress scheduling list according to its deadline interval DI, and that periodically decrement the egress scheduling list deadline interval DI.

93. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly providing voice over packet transmissions and embedded electronic instructions comprising an egress packet control that generates for first and second received packets respective deadline intervals and orders the processing in the processor circuit of the first and second received packets according to the respective deadline intervals.

94. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly providing voice over packet transmissions and embedded

electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the integrated circuit that extract a packet deadline intervals DI, place packets in the egress scheduling list according to deadline intervals DI; and embed a decoder that decodes the packets according to a priority depending to their deadline intervals.

95. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly providing voice over packet transmissions and embedded electronic instructions comprising an ingress/egress packet control that processes egress information and determines lowest first egress deadline interval DI and further executes an ingress process preempting the egress process when the value of lowest first egress deadline interval DI exceeds a predetermined amount K.

96. The wireless telephone of claim 95 further comprising a speech codec coupled to said ingress/egress packet control, and said integrated circuit assembly further comprises a packetizer/depacketizer.

97. The wireless telephone of claim 95 wherein said integrated circuit assembly comprises a digital signal processor and said ingress/egress control includes embedded software instructions executable by said digital signal processor.

98. The wireless telephone of claim 95 further comprising a non-volatile memory storing instructions establishing both a speech codec and said ingress/egress control for

execution by said processor so that said speech codec is controlled by said ingress/egress control.

99. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly providing voice over packet transmissions and embedded electronic instructions comprising an egress packet control establishing an egress scheduling list structure and operations in the integrated circuit that detects whether the arriving packets are respectively voice packets or silence packets, queues information from the voice packets and produces decoded voice information, post-processes the silence packets, and buffers the decoded voice information from the voice packets interspersed with post-processed silence packets.

100. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one integrated circuit assembly generating data descriptive of circular time differences between times of events A and B by electronically subtracting a value representative of the time of event B from a value representative of the time of event A, there resulting a most significant bit (MSB); and providing the MSB itself as a flag indicating which of events A and B is prior to the other.

101. A wireless telephone comprising an antenna, a voice transducer, and at least one integrated circuit assembly coupling the voice transducer to the antenna, said at least one

integrated circuit assembly generating circular time differences between times of events A and B by electronically subtracting and delivering to a storage element a value representative of the time of event B from a value representative of the time of event A, resulting in an electronic representation (delta) having a most significant bit (MSB) and a sign bit S; and electronically processing the electronic representation (delta) and a predetermined value (TMAX) in response to the MSB and the sign bit S to generate the circular time difference.

102. An information storage article of manufacture comprising:

a storage medium holding physical variations representing bits of information; and said bits of information comprising processing instructions for first and second received packets of real-time information, computing for each of said received packets respective deadline intervals; and ordering processing of the first and second received packets according to the respective deadline intervals.

103. The information storage article of manufacture of claim 102 wherein said bits of information further comprise a vocoder coupled to said processing instructions.

104. The information storage article of manufacture of claim 102 further comprising hard disk drive control circuitry assembly and said storage medium including a rotatable hard disk controlled and read by said hard disk drive control circuitry assembly.

105. The information storage article of manufacture of claim 102 wherein said storage medium includes an optically readable surface.

106. The information storage article of manufacture of claim 102 wherein said storage medium includes a magnetically readable surface.

107. The information storage article of manufacture of claim 102 wherein said storage medium includes an integrated circuit memory.

108. A real-time packet networking appliance comprising:

a network interface;

a voice transducer; and

at least one integrated circuit assembly coupling the voice transducer to the network interface, said at least one integrated circuit assembly providing real-time packet transmissions and embedded electronic instructions comprising an egress packet control establishing operations in the processor circuit generating for first and second received packets respective deadline intervals and ordering the processing in the processor circuit of the first and second received packets according to the respective deadline intervals.

109. The real-time packet networking appliance of claim 108 further comprising a speech codec controlled by said egress packet control.

110. The real-time packet networking appliance of claim 108 wherein said speech codec produces frames of encoded and decoded speech and said integrated circuit assembly further comprises a packetizer/depacketizer.

111. The real-time packet networking appliance of claim 108 wherein said integrated circuit assembly comprises a digital signal processor and said egress packet control comprises a block of software instructions executable by said digital signal processor.

112. The real-time packet networking appliance of claim 108 wherein said integrated circuit assembly comprises processor circuitry and a non-volatile memory storing instructions establishing said egress packet control for execution by said processor circuitry.

113. The real-time packet networking appliance of claim 108 further comprising a mobile enclosure holding a user interface coupled to said integrated circuit assembly.

114. The real-time packet networking appliance of claim 108 further comprising a wireless interface unit coupled to said integrated circuit assembly.

115. The real-time packet networking appliance of claim 108 further comprising a modem coupled to said integrated circuit assembly.

116. The real-time packet networking appliance of claim 108 further comprising a wearable mobile enclosure holding a user interface coupled to said integrated circuit assembly.

117. The real-time packet networking appliance of claim 108 further comprising a home appliance enclosure holding a user interface coupled to said integrated circuit assembly.

118. The real-time packet networking appliance of claim 108 further comprising an automotive accessory enclosure holding a user interface coupled to said integrated circuit assembly.

119. The media over packet networking appliance of claim 108 further comprising a compressed-image packet interface coupled to said integrated circuit assembly and an image display coupled to said integrated circuit assembly.

120. A computer comprising

A network interface;

an audio reception transducer;

an audio emission transducer; and

at least one integrated circuit assembly coupling the audio reception transducer and audio emission transducer to the network interface, said at least one integrated circuit

assembly providing voice over packet transmission and reception and including an egress packet control generating for first and second received packets respective deadline intervals and ordering the processing in the processor circuit of the first and second received packets according to the respective deadline intervals.

121. The computer of claim 120 further comprising an audio codec controlled by said egress packet control.

122. The computer of claim 120 wherein said audio codec produces and receives frames of encoded audio and said integrated circuit assembly further comprises a packetizer and depacketizer responsive to the frames to output and receive packets including at least one frames in a packet.

123. The computer of claim 120 wherein said integrated circuit assembly comprises a digital signal processor.

124. The computer of claim 120 wherein said integrated circuit assembly further comprises a non-volatile memory storing instructions establishing said egress packet control for execution by said digital signal processor.

125. A private branch exchange comprising

telephone interface circuitry having plural connectors ready for connection to plural telephone units;

a digital network interface ready for connection to PSTN (public switched telephone network); and

at least one integrated circuit assembly coupling the telephone interface circuitry to the digital network interface, said at least one integrated circuit assembly providing voice over packet transmission and reception and including egress packet control of voice packets generating for first and second received packets respective deadline intervals and ordering the processing in the integrated circuit assembly of the first and second received packets according to the respective deadline intervals.

126. A wireless base station comprising

cellular telephone wireless transmit/receive interface circuitry for communication with cell telephone handsets in the vicinity of the wireless base station;

a packet network interface; and

at least one integrated circuit assembly coupling the cellular telephone wireless transmit/receive interface circuitry to the packet network interface, said at least one integrated circuit assembly providing voice over packet transmission and reception and including an egress packet control of voice packets generating for first and second received packets respective deadline intervals and ordering the processing in the integrated circuit assembly of the first and second received packets according to the respective deadline intervals.

127. A computer add-in card comprising:

a processor circuit;

an egress packet control generating for first and second received packets respective deadline intervals and ordering the processing in the integrated circuit assembly of the first and second received packets according to the respective deadline intervals;

a printed wiring board bearing said processor circuit and egress packet control, said printed wiring board having an output connector for passage of packets and diversity packets therethrough from said processor and said printed wiring board further having an insertion connector, whereby the printed wiring board is insertable via the insertion connector.

128. The computer add-in card of claim 127 further comprising a speech codec coupled to said egress packet control.

129. The computer add-in card of claim 127 wherein said speech codec produces frames of encoded speech and said integrated circuit further comprises a depacketizer coupled between said egress packet control and said connector.

130. The computer add-in card of claim 127 wherein said processor circuit comprises a digital signal processor multiplier and arithmetic logic unit.

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